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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/064,474 04/22/98 ROY

S TRA-040

EXAMINER

LM01/0610

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65 WOODS END ROAD
STAMFORD CT 06905

WHITMORE, S

ART UNIT

PAPER NUMBER

2786
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/064,474

Applicant(s)
Subhash et al.

Examiner
Stacy Whitmore

Group Art Unit
2783



☒ Responsive to communication(s) filed on Apr 22, 1998

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-25 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-25 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-25 are presented for examination.
2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.
3. It is noted that the present application does not contain line numbers in the specification of claims, and does not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the Examiner and Applicant all future correspondence should include the recommended numbering.

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Folwell et al. (5,473,754) in view of

6. As for claim 1, Folwell et al. taught the invention substantially as claimed, including a processor having a real time debugging interface (abstract), comprising:

- a) instruction memory means (fig. 2 element 21),
- b) program counter means (col. 5 lines 4-5),
- c) cause register means for indicating information regarding interrupts and exceptions (col. 5 lines 1-10, and Table 4), and
- d) first decoder means for indicating information about an instruction executed by the processor during a clock cycle (fig. 2 element 22), the first decoder coupled to the instruction memory, the program counter and the cause register, where the first decoder has a first output providing information regarding activity of the processor (fig. 2 elements 24 and 26, col. 1 lines 62-67, col. 2 lines 1-4).

Folwell et al. does not specifically teach the decoder operating in real time. However, Folwell et al. Did disclose the decoder operating directly with instruction

flow and the debug port, both of which operate in real time. It would have been obvious for one of ordinary skill in the art at the time the invention was made that Folwell et al.'s decoder operates in real time because it is part of normal program operation which operates in real time.

7. As for claim 11, Folwell et al. taught the invention substantially as claimed, including the limitations as cited in claim 1. Folwell et al. Did not specifically disclose plural elements within an embedded system. However, Folwell et al. disclosed his debug device coupled to a host work station via a SCSI bus (fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a plurality of elements in an embedded system into Folwell et al.'s system because Folwell et al.'s system was expandable via the SCSI.

8. As for claim 21, Folwell et al. taught a method of debugging a processor comprising:

- a) providing information about processor activity in real time (abstract), and
- b) associating the instructions executed by the processor with information about processor activity (col. 5 lines 52-53).

9. As for claims 2, 12, and 24, Folwell et al. taught the information about processor activity includes information as to at least one of a jump instruction has

been executed (col. 2 table 3), a jump instruction based on the contents of a register has been executed (col. 2 table 3), a branch has been taken (col. 2 table 2), and an exception has been encountered (col. 5 table 4).

10. As for claims 3, 13 and 22, Folwell et al. taught the clock cycle is a processor clock cycle (col. 1 lines 34-36), and

the first decoder updates the information about each instruction executed by the processor for each of the processor clock cycles (col. 1 lines 5-9, and 34-36).

11. As for claims 4, 14 and 23, Folwell et al. taught the information about each instruction executed by the processor includes an indication whether or not an instruction has been executed since a previous processor cycle (col. 1 line 62 - col. 2 line 4).

12. As for claims 5 and 15, Folwell et al. did not specifically teach the first output is a three bit parallel output. However, Folwell et al. disclosed a parallel output of more than three bits (fig. 2 elements 24 and 26). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Folwell et al.'s performed the same function as claimed by applicant because Folwell et al.'s parallel output included at least three bits of information and could have been designed to use three bits as an output.

13. As for claims 6 and 16, Folwell et al. did not expressly teach

e) second decoder means, and

f) event history buffer means

as coupled together as claimed by applicant.

However, Folwell et al. disclosed

e) a second decoder means coupled to the cause register for indicating information about the contents of cause registers, and having a second output, and enables the event history buffer to capture contents of the cause register when a particular event is indicated. (col. 5 lines 8-27, and col. 7 line 60 - col. 8 lines 11)

f) event history buffer means for storing information regarding processor events (col. 5 lines 8-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made that although Folwell et al.'s system was not coupled exactly as claimed, it performed the same function as applicant's claimed limitations.

14. As for claims 7, 17 and 25, Folwell et al. disclosed the second decoder means enables the event history buffer means when the cause register means indicate an event of a change in status of an interrupt line, internal processor exception, or a

jump based on the contents of a register (col. 1 line 64 - col. 2 line 3, and col. 8 lines 1 - 9).

15. As for claims 8 and 18, Folwell et al. did not specifically teach the event history buffer is a bit serial output. However, Folwell et al. disclosed the output FIFO (col. 8 line 9), which could be configured to have a serial output.

16. As for claims 9 and 19, Folwell et al. disclosed the processor is on a chip having a plurality of pins (col. 1 lines 5-9), and the first output and data output are provided via some of the pins (fig. 1 element 25 and fig. 2 element 26).

17. As for claims 10 and 20, Folwell et al. disclosed the first output is an n-bit parallel output (fig. 2 element 26), and the data output is a serial output (see as cited in paragraph 15).

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Harenberg et al.	5,544,311	debug port, real-time
Argade et al.	5,724,505	debug host, real-time
Dewitt et al.	5,572,672	monitor in real-time

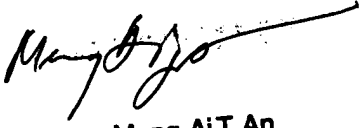
19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Stacy Whitmore, whose telephone

number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday and alternate Fridays from 6:30AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Meng Ai T. An*, can be reached on (703) 305-9678.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Stacy Whitmore
Jun 3, 1999


Meng-Ai T. An
Supervisory Patent Examiner
Technology Center 2700